

5A, 600V N-CHANNEL MOSFET

GENERAL DESCRIPTION

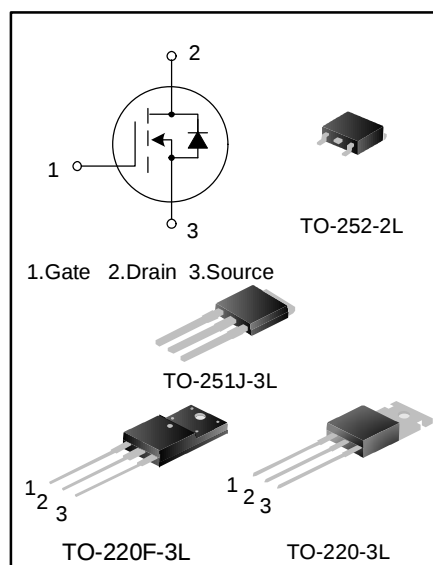
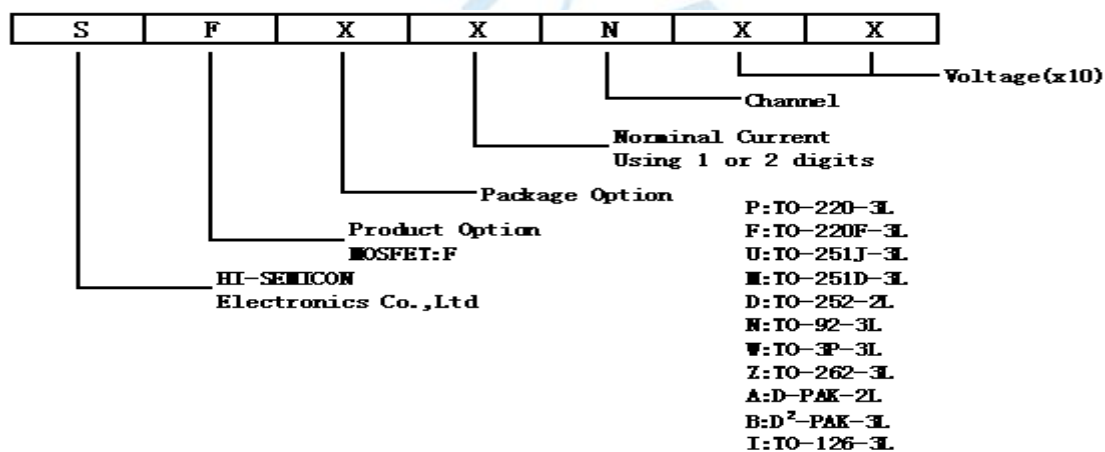
This power mosfet is an N-channel enhancement mode power MOS field effect transistor which is produced using Hi-semicon proprietary F-Cell™ structure VDMOS technology. The improved planar stripe cell and the improved guard ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.

FEATURES

- ◆ 5A, 600V, $R_{DS(on)}$ (typ) = 1.88Ω @ $V_{GS}=10V$
- ◆ Low gate charge
- ◆ Low C_{rss}
- ◆ Fast switching
- ◆ Improved dv/dt capability

NOMENCLATURE



ORDERING INFORMATION

Part No.	Package	Marking	Material	Packing
SFP5N60	TO-220-3L	SFP5N60	Pb free	Tube
SFF5N60	TO-220F-3L	SFF5N60	Pb free	Tube
SFD5N65	TO-252-2L	SFD5N65	Pb free	Tape & Reel
SFU5N60	TO-251J-3L	SFU5N60	Pb free	Tube

ABSOLUTE MAXIMUM RATINGS ($T_c=25^{\circ}\text{C}$ unless otherwise noted)

Characteristics		Symbol	Ratings		Unit
			SFP/U/D5N60	SFF5N60	
Drain-Source Voltage		V _{DS}	600		V
Gate-Source Voltage		V _{GS}	±30		V
Drain Current	T _C =25°C	I _D	5		A
	T _C =100°C		3.1		
Drain Current Pulsed		I _{DM}	20		A
Power Dissipation(T _C =25°C) -Derate above 25°C		P _D	120	40	W
			0.96	0.32	W/°C
Single Pulsed Avalanche Energy (Note 1)		E _{AS}	242		mJ
Operation Junction Temperature Range		T _J	-55~+150		°C
Storage Temperature Range		T _{sta}	-55~+150		°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings				Unit
		SFP5N60	SFD5N60	SFU5N60	SFF5N60	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.04	1.04	1.00	3.13	$^{\circ}\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	110	110	120	$^{\circ}\text{C/W}$

ELECTRICAL CHARACTERISTICS ($T_c=25^{\circ}\text{C}$ unless otherwise noted)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	$B_{V_{DS}}$	$V_{GS}=0V, I_D=250\mu A$	600	--	--	V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=600V, V_{GS}=0V$	--	--	1.0	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 30V, V_{DS}=0V$	--	--	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=2.5A$	--	1.88	2.15	Ω
Input Capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V, f=1.0\text{MHz}$	--	479.8	--	pF
Output Capacitance	C_{oss}		--	62.7	--	
Reverse Transfer Capacitance	C_{rss}		--	2.1	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=300V, I_D=5.0A, R_G=25\Omega$ (Note 2,3)	--	14.93	--	ns
Turn-on Rise Time	t_r		--	28.40	--	
Turn-off Delay Time	$t_{d(off)}$		--	28.27	--	
Turn-off Fall Time	t_f		--	21.73	--	
Total Gate Charge	Q_g	$V_{DS}=480V, I_D=5.0A, V_{GS}=10V$ (Note 2,3)	--	9.27	--	nC
Gate-Source Charge	Q_{gs}		--	2.79	--	
Gate-Drain Charge	Q_{gd}		--	3.37	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	5	A
Pulsed Source Current	I_{SM}		--	--	20	
Diode Forward Voltage	V_{SD}	$I_S=5.0A, V_{GS}=0V$	--	--	1.4	V
Reverse Recovery Time	T_{rr}	$I_S=5.0A, V_{GS}=0V,$ $dI_F/dt=100A/\mu s$	--	459.99	--	ns
Reverse Recovery Charge	Q_{rr}		--	2.3	--	μC

Notes:

1. $L=30\text{ mH}$, $I_{AS}=3.78A$, $V_{DD}=70V$, $R_G=25\Omega$, starting $T_J=25^\circ C$;
2. Pulse Test: Pulse width $\leq 300\mu s$, Duty cycles $\leq 2\%$;
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

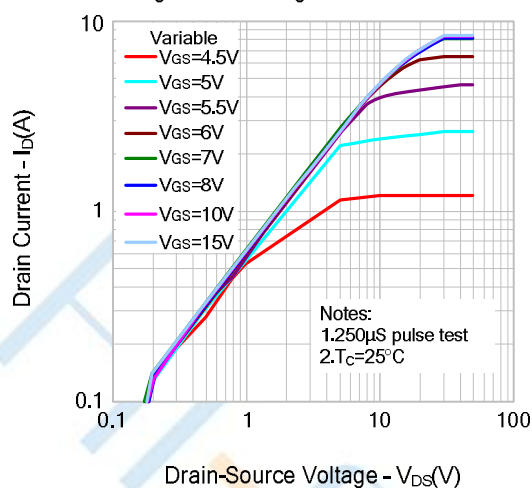


Figure 2. Transfer Characteristics

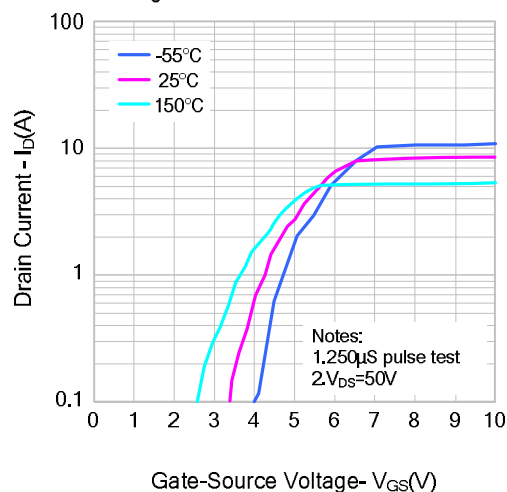


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

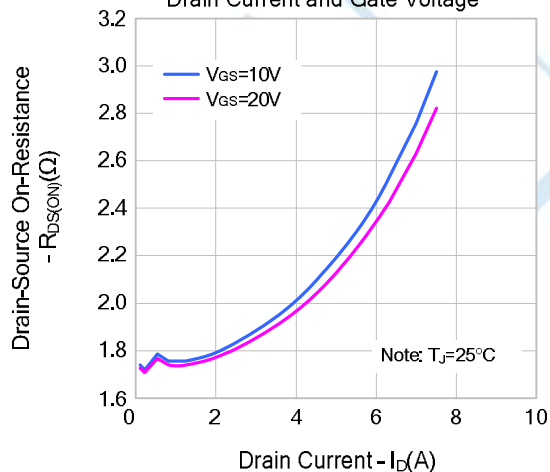


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

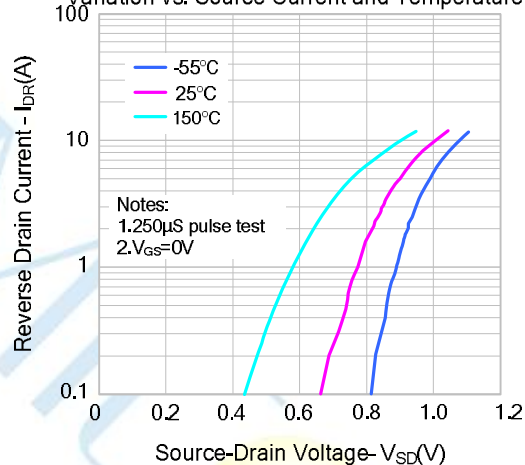


Figure 5. Capacitance Characteristics

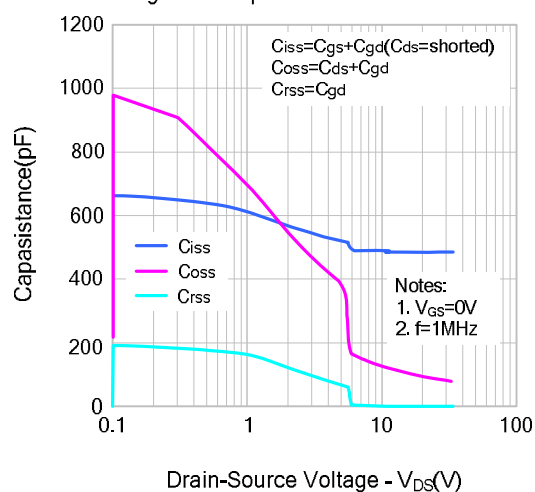
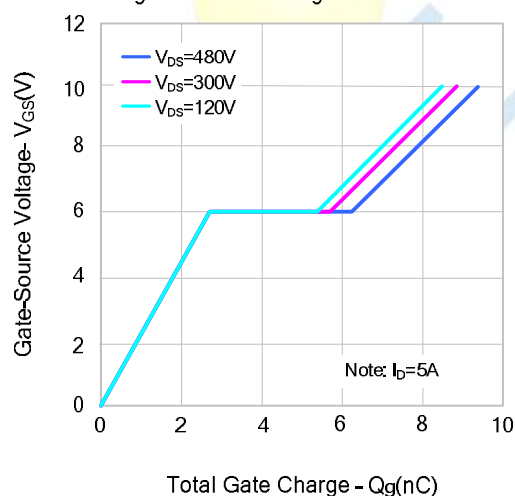


Figure 6. Gate Charge Characteristics



TYPICAL CHARACTERISTICS(continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

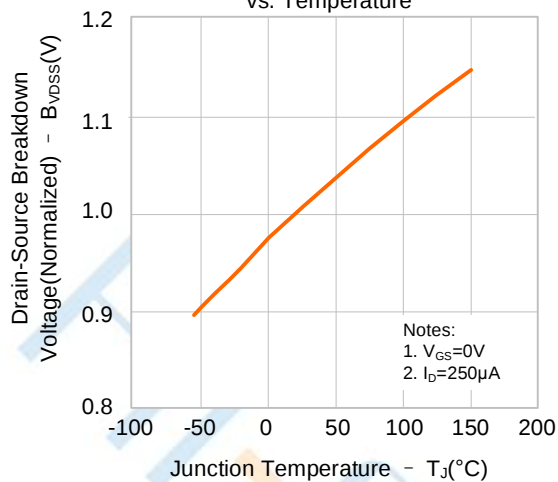


Figure 8. On-resistance Variation vs. Temperature

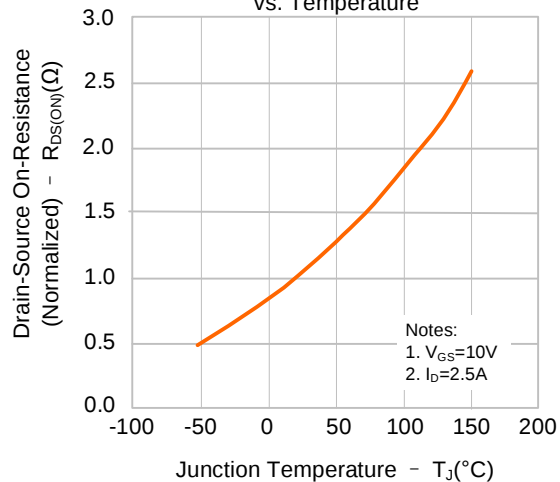


Figure 9-1. Max. Safe Operating Area (SFU/D/P5N60)

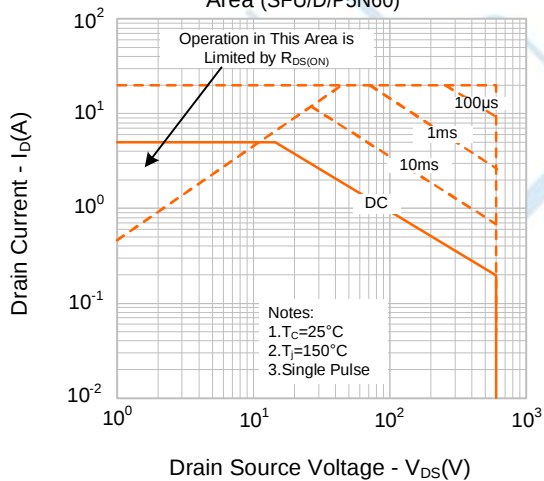


Figure 9-2. Max. Safe Operating Area(SFF5N60)

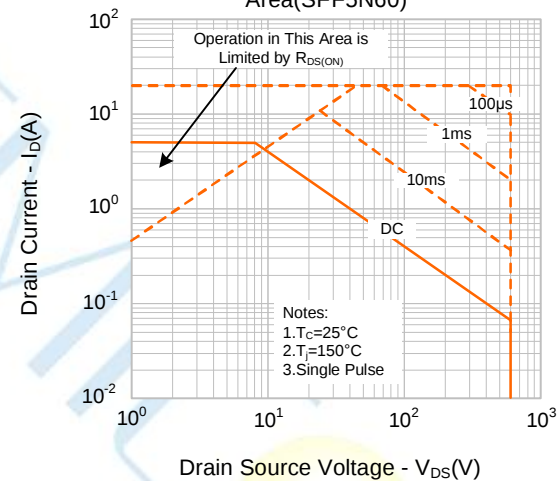
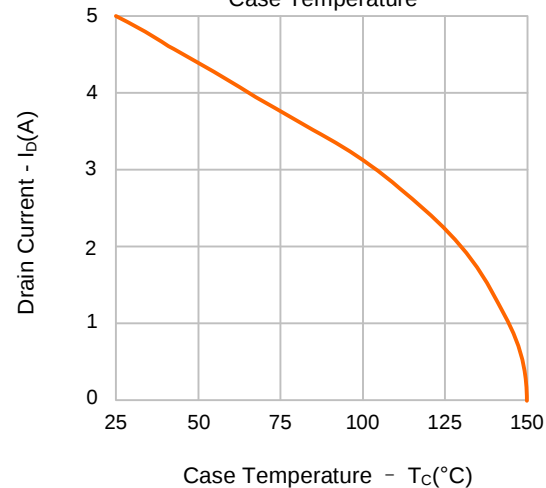
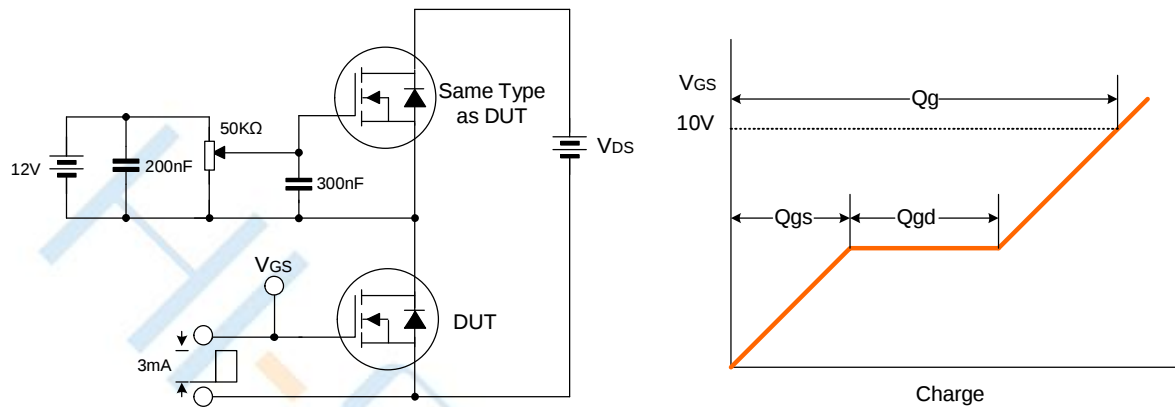


Figure 10. Maximum Drain Current vs. Case Temperature

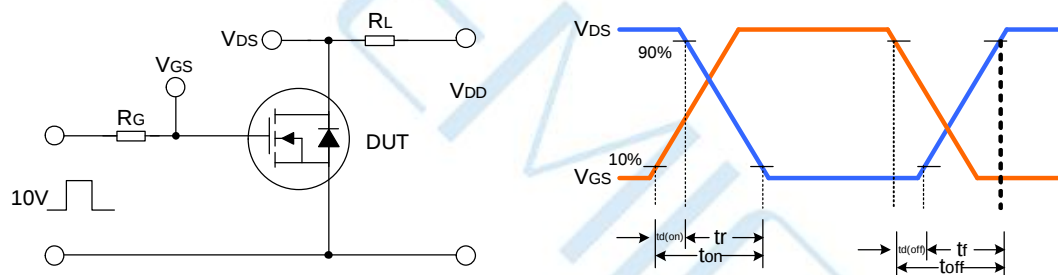


TYPICAL TEST CIRCUIT

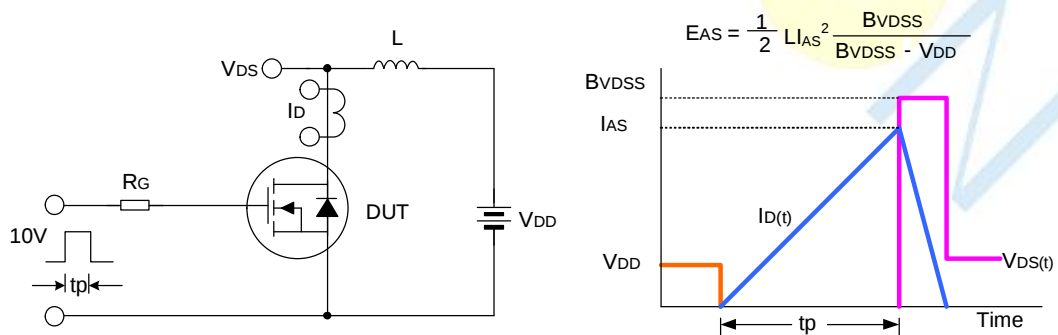
Gate Charge Test Circuit & Waveform



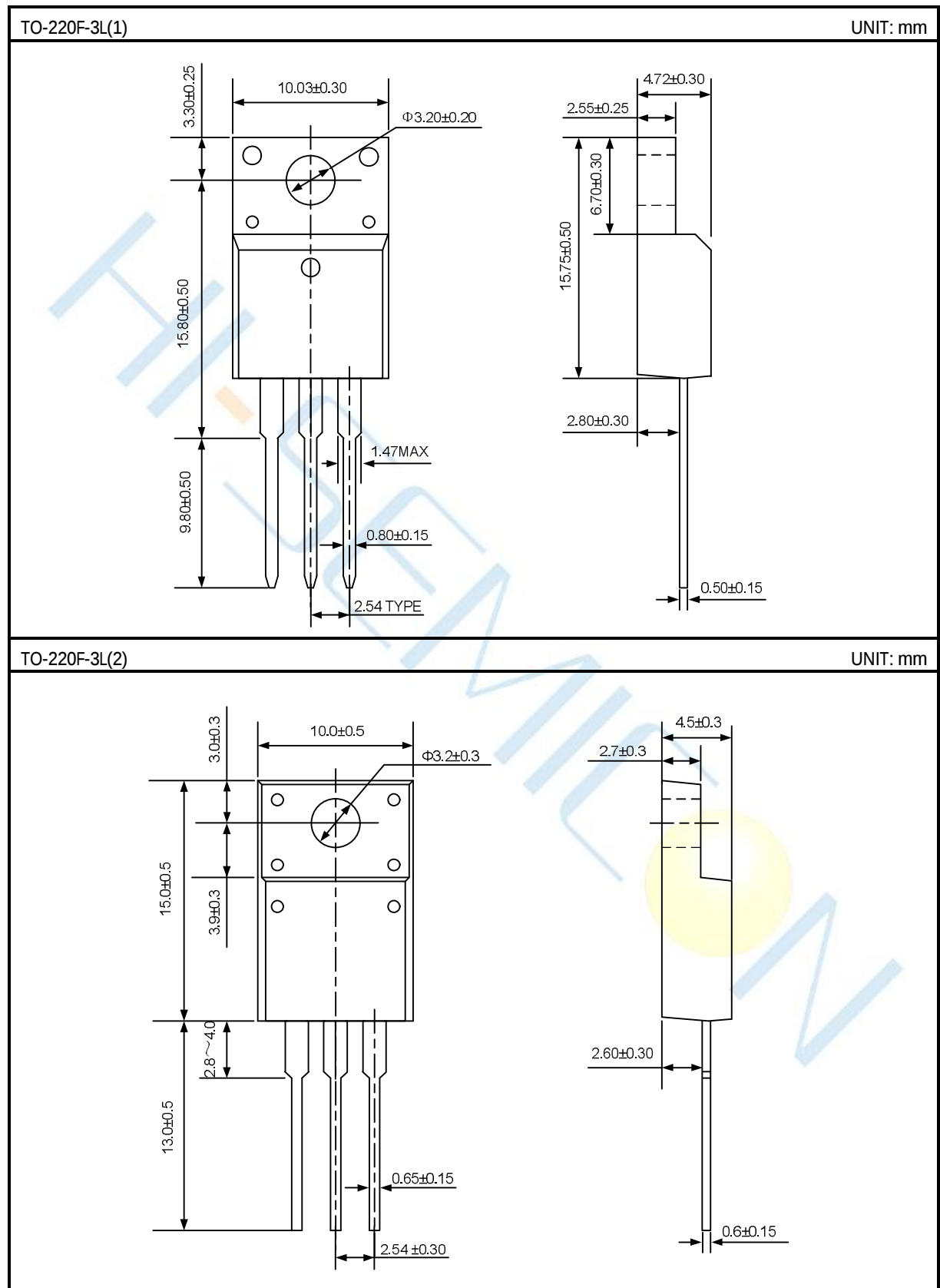
Resistive Switching Test Circuit & Waveform



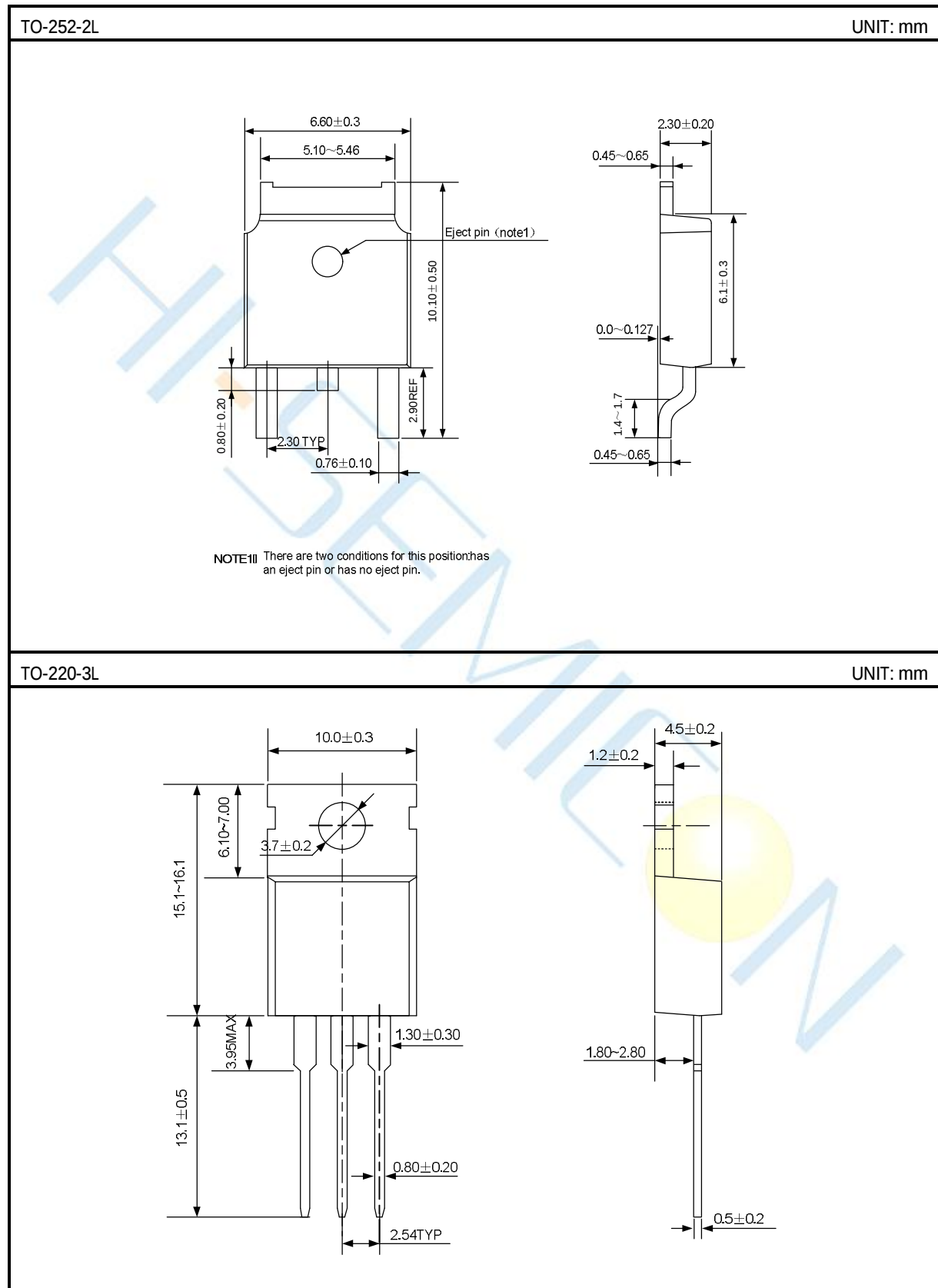
Unclamped Inductive Switching Test Circuit & Waveform



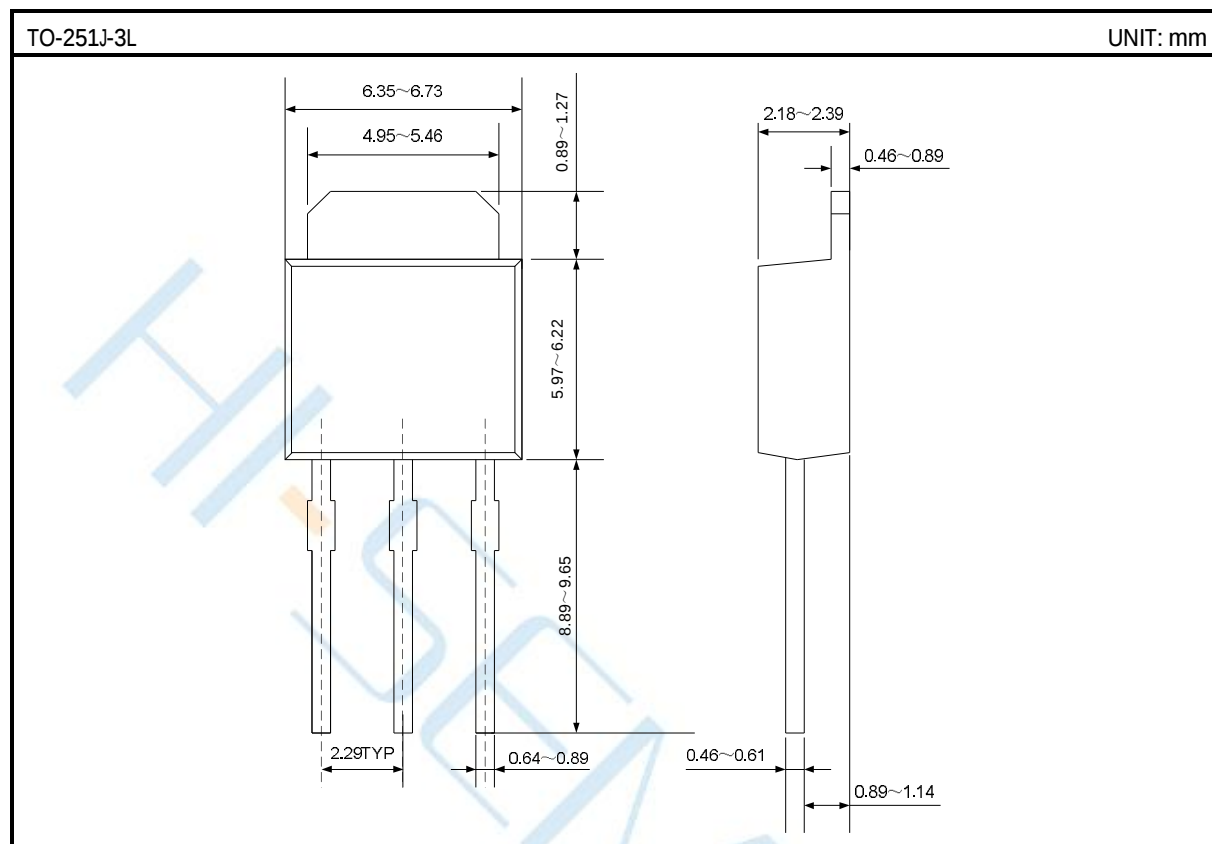
PACKAGE OUTLINE



PACKAGE OUTLINE (continued)



PACKAGE OUTLINE (continued)



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- Hi-semicon will supply the best possible product for customers!